APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,351	07/03/2001	Pratap Subrahmanyam	10991880	1056

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EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
		09/898,351	SUBRAHMANYAM ET AL.
Office Action Summary		Examiner	Art Unit	
		Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>20 June 2005</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1,2,4-12,14-17,19 and 20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1,2,4-12,14-17,19 and 20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's Appeal Brief filed 6/20/2005.

Claims 1-2, 4-12, 14-17, 19-20 are pending in the office action.

After review of the arguments by Applicants presented in the Appeal Brief and the

rationale of the rejection in light of the prior art of references, the prosecution of the case is now

RE-OPENED.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1-2, 4-12, 14-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Wu, USPN: 6,668,372 (hereinafter Wu), in view of Holmberg et al., USPubN:

2001/0021959 (hereinafter Holmberg) and further in view of Burke et al., 6,738,865 (hereinafter

Burton).

As per claim 1, Wu discloses a method to analyze a computer program that includes a

plurality of block of code, the method comprising :

receiving a block of code instruction in memory (e.g. Fig. 1; col. 26 lines 26-36);

using a counter for tracking each time said code instruction is loaded for execution (e.g.

col.3, lines 37-53; Fig. 2A-B);

maintaining a counter for storing each said counter of said block code (e.g. Fig. 2A-B)

while said code instruction is stored on said code memory;

and maintaining of a storage area for storing each said counter of said block of said

block previously executed (e.g. Fig. 2a, 3).

But Wu does not explicitly disclose that said code memory is code cache nor does Wu

disclose that the counter is maintained in a cache. In a same endeavor as to applying execution

profiling analogous to Wu, Holmberg discloses basic blocks execution code cache (para 0028,

0034-0036) and counter cache (e.g. *reference number 23, counter 25* – Fig. 1a). Based on the

known concept as to use cache to alleviate memory access time and the rationale as to why fast

memory resources should be optimized in regard to what is to be stored therein, as indicated

from the need to have profiling measurements by both Wu and Holmberg (see Holmberg:

BACKGROUND, para 0005-0006), it would have been obvious for one of ordinary skill in the

art at the time the invention was made to enable the Wu's execution environment so that code

blocks or instructions are loaded into cache and that counter be implemented as entities also

being cached (counter cache) because according to Holmberg this would alleviate access time

and enable dynamic and flexibility in updating profile measurements (pg. 2, para 0013-0015).

Nor does Wu explicitly disclose maintaining storage said counter after said block of

code is evicted from code cache. Tracking code execution frequency via analysis of profiling as

taught by Wu and Holmberg is furthered by Burton which optimizes the use of fast memory with

LRU policy and teaches a cached counter to tracking priority levels of code execution (see *LRU,*

cache, counter 18 – Fig. 1; see Fig. 2-3). Based on known concept as to why cache replacement

is so frequently used such as via LRU by Burton, which is another form of a common endeavor

as to optimizing resources of fast memory as presented by Holmberg and Wu's profiling

execution, it would have been obvious for one of ordinary skill in the art at the time the invention

was made to provide such tracking of execution frequency as taught by Wu or Holmberg so that

the frequency counter as shown by Wu is maintained after the block of code least executed is

evicted from the LRU policy as by Burton, since a maintained piece of information about the

frequency of the most or least recently executed instructions would direct how the cache

replacement as purported by Burke would successfully operate for subsequent operations dealing

with cache replacement and thereby cache storage would be salvaged (see Burton

BACKGROUND, and Summary).

As per claim 2, based on the known concept to apply LRU policy to prevent cache over

storage, the teachings by Wu to discard data when a memory size is exceeded (see Wu, col. 14,

lines 20-21); or profiling by Wu as combined with Holmberg, the desirability to keep the code

cache from being full is recognized. Further, Burton discloses such concept of determining

whether a cache is full (see *LRU, threshold* - Fig. 3). It would have been obvious for one of

ordinary skill in the art at the time the invention was made to provide the additional step of the

cache threshold determining as taught by Burton to the method of Wu/Holmberg, because

providing a replacement policy to alleviate burden of a cache requires means of finding when

cache resources reach unwanted threshold as shown by Burton or implied by well-known

methodology to apply LRU replacement to avert storage exceeding as from above, because there

would be no need to apply a replacement algorithm when no resources are threatened.

As per claim 4, the combination of Wu/Holmbert/Burton discloses determining which of

said counter of said block of code stored on said counter cache is least recently executed; and

further teaches evicting said least recently executed block of code related to said counter from

said code cache (re claim 1 and the LRU related teachings by Burton). Further, the rationale as

to combine the record of demoted entries by Burton in conjunction with the profiling execution

by Wu/Holmberg along with discarding of data when a memory size is exceeded (see Wu, col.

14, lines 20-21) has rendered obvious the limitation as to copying said counter of said least

recently executed block of code from said counter cache to said storage area when said least

recently executed block of code related to said counter is evicted from said code cache (re

corresponding rejection in claim 1) because a counter being persisted in a memory area would

continue to provide information in support of the cache replacement policy to operate.

As per claim 5, Wu (in combination with Holmberg) discloses

checking said storage area to determine if said block of code is being executed for other

than the first time; loading said counter associated with said block of code being executed for

other than the first time; and updating said counter associated with said block of code being

executed for other than the first time (Note: Re claim 1 - the instituting of a counter is to keep

track with a code block is being executed every time – including second time -- for its count to

be updated in the counter ; and the fact that a number being incremented from x to x+1 for

example implicitly teaches checking whether if said block is being executed other than time x).

As per claim 6, Wu discloses a method to analyze a computer program that includes a

plurality of blocks of code, the method comprising means for:

executing said computer program; counting one of said plurality of blocks is executed

(e.g. Fig. 2A-B);

maintaining a counter for storing said plurality of counting means of said plurality of

blocks that are executed (e.g. Fig. 2-3 -- Note: maintaining a counter associated with a cache for

storing said plurality of count references in a cache of said blocks of code that are most recently

executed);

maintaining a counter in a storage area for storing said counting means of said blocks of

code that are executed (e.g. Fig. 2-3).

But Wu does not disclose maintaining a counter cache for storing the counting means.

This limitation as to store instructions in cache or a counter in cache has been addressed in claim

1 using Holmberg.

Nor does Wu disclose counter is for counting block of codes that are the most recently

executed; but based on the demotion of code that are not executed frequently, the least recently

executed – LRU – policy as disclosed by Burton in light of the rationale in claim 1, this

limitation would have been obvious because of the endeavor to alleviate processor memory

resources and optimize the use of fast memory as purported by the profiling execution by Wu

and Holmberg as set forth in claim 1 above.

As per claim 7, this limitation is rejected using the same rationale as set forth in claim 2.

As per claim 8, in view of the techniques taught by Burton (see pg. 7, para 0080) and the

rationale in claim 7, the limitation of copying blocks from counter cache to a storage area when

the counter cache is full would also be obvious in light of the knowledge on why a LRU is used

and Burton's teachings (see Burton: *storage 6* - Fig. 3; col. 4, lines 6-34). One skill in the art

would apply storing away the least used data to a storage when the cache threshold is threatened

as taught by well-known practices or Burton's demoting as by Burton in light of Wu's discarding

of excess data and Holmberg's technique to keep the most used data in fast memory because of

the same reasons as to why counter and code should be evicted or stored away from fast memory

to salvage storage resources therein as set forth in claim 1.

As per claim 9, Wu teaches counting of most frequently executed code blocks (Fig. 2-3)

and Holmberg teaches maintaining in cache the most frequently executed data and keep less used

data in a slower memory (pg. 5, para 0050; pg. 7, para 0080) while Burton teaches cache

recording of LRU(least recently used) information (Fig. 2) in conjunction with demoting cache

entries so they are stored into secondary area (re claim 1, 2). The limitation as to determining

which of the counting means of code blocks is least recently used and copying said block of code

to a storage area when the cache is full would also have been obvious using the rationale as set

forth in claim 8 above.

As per claim 10, this claim includes limitation of claim 5 and is rejected using the

corresponding rationale as set forth in claim 5.

As per claim 11, this is a computer readable medium having computer readable program

code embodied therein to perform when executed a method for analyzing a computer program

that includes a plurality of blocks of code comprising logic to perform the same steps as recited

in claim 1; hence is rejected with the corresponding rejection as set forth therein.

As per claims 12, 14, and 15, these claims correspond to claims 2, 4, and 5, respectively;

hence are rejected using the corresponding rejections as set forth therein.

As per claim 16, this claim is the system version of claim 1, hence is rejected with the

corresponding rejection as set forth therein.

As per claims 17, 19, and 20, these claims correspond to claims 2, 4, and 5, respectively;

hence are rejected using the corresponding rejections as set forth therein

Response to Arguments

4.   Applicant's arguments with respect to claims 1-2, 4-12, 14-17, 19-20 as presented in the

Appeal Brief have been considered but for the most part are moot in view of the new ground(s)

of rejection. That is, Wu is herein used to address keeping track with frequency of block of code

execution in a profiling execution; Holmberg is used to teach code cache and counter cache to

enhance resource optimization and profiling by Wu; and Burton is to teach LRU policy with

demoting of least frequently executed code and evicting with counter tracking in support thereto.

Conclusion

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (571)272-3719.

        The fax phone number for the organization where this application or proceeding is

assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before

using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-
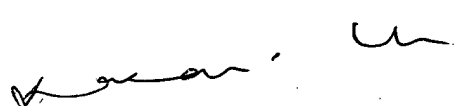
272-3609.

        Any inquiry of a general nature or relating to the status of this application should be

directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
September 17, 2005

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